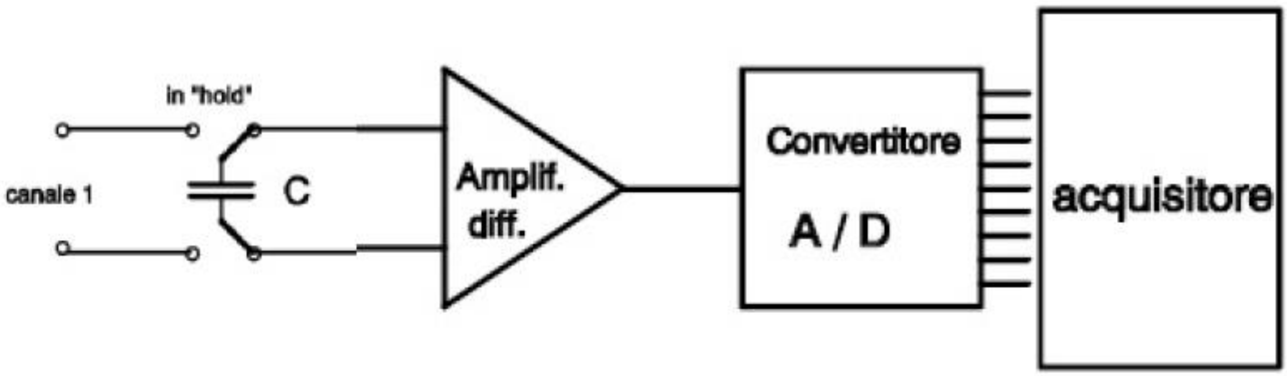
Industrial Informatics and Embedded Systems (Embedded) - *May 5th 2009*

Surname ....….. Name .... Registration n° …………………………

1. Design a 14 bits dual slope ADC considering a 1 MHz clock and a reference voltage equal to 1 V. The signal to be converted is included within 0V and 10V. To this aim size properly the necessary impedances in the circuit so to avoid the amplifiers saturation. Calculate the conversion times.



If the ADC belongs to a measurement chain as the one shown in the figure, estimate the repetition time of the polling routine executed on the microprocessor that manages the sample and hold unit, program the amplifier gain and starts the conversion.

2. It is required to measure the frequency produced by a pulse signal with a frequency range variable in [5 MHz … 80 MHz] usig a 16 bit microprocessor.

- Describe how the chosen technique works so as to minimise the uncertainty range in the worst case; it is allowed to assume that the interruptn service latency (if necessary) is 1 nsec
- Verify that the constraints of the chosen technique are satisfied
- Determine the maximum and minimum frequencies at now measurable with the set constraints

3. Implement a filter that is ruled by the following expression:

$$U(k)=I(k) + CF*[U(k-1)-I(k)]$$

where CF=0.75, U(k) is the present output of the filter and I(k) the input at the k^{th} sampling time.
Assume that it is possible to use a 16 bits microprocessor without floating point unit.
Show a cycle of the software routine implemented when U(k)=35, RESTO(k)=0.1875 and I(k)=30.
Provide an estimation of the time after which the output reaches the input value.

4. Illustrate the issues related to the measurement phase when the read datum must be transformed by the microprocessor in the corresponding value of the physical magnitude acquired by the transducer

MAY 5TH 2009

EX 2

|SW SW| NO $T_c < \frac{1}{2f_{max}} = 6\mu sec$ $T_c \cong 50-100\ cc$ $1\ cc\ (\text{clockcycle}) = \frac{6\ 10^{-9}}{50-100} = 1.2\ 10^{-8} \div 6\ 10^{-11}$ feasible?

|HW INT| $f_{max}\,\Delta T < 2^N$ $\Delta T = \frac{2^{16}}{80\ 10^6} = 0.8\ 10^{-3}\,s$ & $f_{min} > \frac{1}{\Delta T}$ $\Delta T > 0.2\ 10^{-6}$ ALWAYS CHOSE ΔT_{MAX} SINCE ASSURES MORE ACCURACY

$$Er_{min|max} = \pm\left(\frac{1}{f_{min}\,\Delta T} + \frac{T_{LAT}}{\Delta T}\right) = \pm\left(\frac{1}{5\,10^6 \cdot 0.8\,10^{-3}} + \frac{10^{-9}}{0.8\,10^{-3}}\right) = 0.25\ 10^{-3}$$

|HW HW| IN THIS CASE LET'S ASSUME THAT THE RSET AND INTREQ BITS ARE SENT TO THE PORT

$$\Delta T = \frac{2^{N-2}}{80\,MHz} \leq 0.2\ 10^{-3} \quad \text{AND AS BEFORE} \quad \Delta T \geq \frac{1}{f_{min}} \geq 0.2\ 10^{-6}$$

$$Er_{min} = -\left(+\frac{T_{CK}}{\Delta T} + \frac{1}{f_{min}\,\Delta T}\right) = -\left(\frac{T_{CK}}{\Delta T} + \frac{1}{5\,10^6\ 0.2\,10^{-3}}\right) = -\left(\frac{T_{CK}}{\Delta T} + 10^{-3}\right)$$

$T_{CK}\,2^k = \Delta T$ $\frac{T_{CK}}{\Delta T} \leq 10^{-3}$ $k \approx 10$

$$Er_{sup} = \frac{1}{f_{min}\,\Delta T} = 10^{-3}$$

|2INP| $T_{CK} > \frac{1}{2^N f_{min}}$ $T_{CK} > 6.1\ 10^{-12}$ $T_{CK} < \frac{1}{f_{max}} < 1.25\ 10^{-8}$ $6\ 10^{-12} < T_{CK} < 125\,\mu sec$

$$Er_{inf} = -\frac{f_{max}(T_{CK} + T_{LAT})}{1 + f_{max}(T_{CK} + T_{LAT})} = \text{REASONABLE } T_{CK} = 1\,\mu sec = -\frac{80\,10^6 \cdot 2\,10^{9}}{1 + 80\,10^6 \cdot 2\,10^{9}} = -0.138 \sim 14\%$$

$$Er_{sup} = \frac{f_{max}(T_{CK} + T_{LAT})}{1 - f_{max}(T_{CK} + T_{LAT})} = 0.19 \sim 19\%$$

BEST HW INT REAL $f_{max} = \frac{2^N}{\Delta T} = \frac{2^{16}}{0.8\,10^{-3}}$ $f_{min} = \frac{1}{\Delta T}$