Industrial Informatics and Embedded Systems (Embedded) - *May 19th 2020*

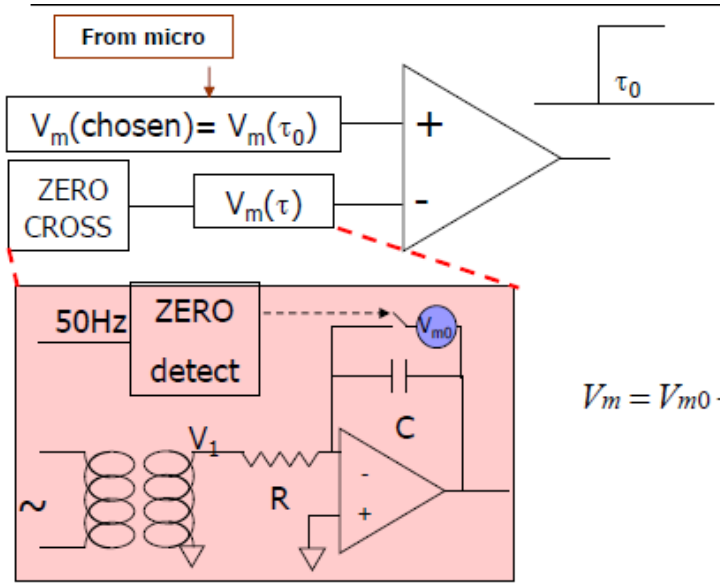
Surname ……. Name ……. Registration n° ……

Time for delivery (tight): 6 pm

1. Consider the following assembly code and identify the general function developed if it exists. Then translate it into ARM assembly language

```
        mov r3, #31
        r2, #0
loop:   mov r2, r2, lsl #1
        cmp r1, r0, lsr r3
        suble r0, r0, r1, lsl r3
        addle r2, r2, # 1
        subs r3, r3, # 1
        bge loop
        mov r1, r2
        mov pc, lr
```

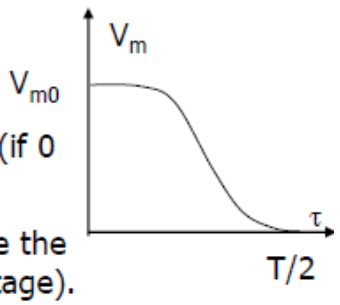
2. Briefly answer to the following questions:
   - What is the transfer function that should be emulated by the SCR emulator in case of inductive load?



From the μP we set the chosen V_m (related to the desired power), so as when the corresponding τ is reached the comparator exits a pulse to power up the SCR.

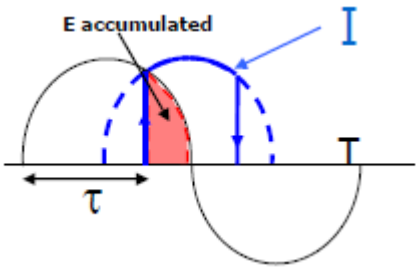
How to generate $V_m(\tau)$?

$$V_m = V_{m0} - \int_0^{\tau} \frac{V_1}{RC} dt \qquad V_{m0} = \int_0^{T/2} \frac{V_1}{RC} dt$$



By setting $V_m(\tau_0)$ from the μP the load voltage can be regulated (if 0 null power if V_{m0} max. power)

As an alternative a suitable lookup table in μP memory can relate the power delay (t) with the corresponding average load power (voltage).

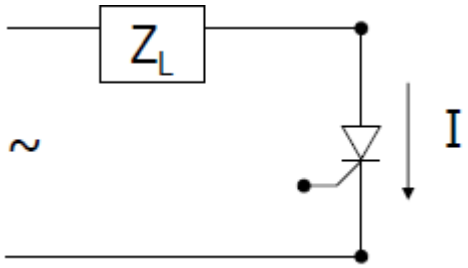


$$I = \int_{\tau}^{t_{spegnim}} \frac{V_p}{L} sen\, \omega t\, dt$$

The picture shows the emulator when the load is inductive.

If the load is inductive the same idea can be maintained considering however that we have to reproduce the current crossing an inductor like shown by this expression where tspegnimento is = T-τ.

Therefore the circuit can be designed like this one



with a resistor replacing the SCR. The voltage taken at the extremities of the resistor will be the Vm value that must be inserted the "-" input of the operational amplifier.

- During a marathon the athletes pass close to many detection points that are displaced along the track every km. The athlete number is transmitted from the detection point (probably equipped with a powerful microprocessor) in the same format as Can but exploiting the 4G technology, to a central computer that monitors the race and provides statistics and estimations. If the number of the athletes can reach 100, what are the maximum and minimum frequencies of the information that are received by the central computer?

Let' suppose that the identifier of the athlete is a byte (100 athletes is ok) and let's suppose that the worst case is when all the 100 athletes contemporaneously arrive at the check point while the best case is when only one arrives at the check point and in both the cases their information must be sent to the central computer before the athletes arrive at the next check point.

If we assume a velocity for the athletes equal to 5 km/h this means that we have three minutes for sending all the information before the next check point is reached.

If we use Can protocol the protocol asks for a RF + IF + DF that is 44 bits + 3 bits + 52 bits (if identifiers with 11 bit are sent) assuming no error passive node and no Bus Idle sequence in the IF frame.

Therefore the number of the bits that must be received is in the worst case 100*99 and 99 in the best one. Assuming that the velocity of the Can bus is 1 Mb/sec the time necessary in the two cases is 9,9 msec and 99 microsec well below the time limit found before.

- Why the management of a Fast Interrupt is faster and lighter than the normal IRQ service in ARM?

See slide 109 in the "Embedded systems" section.

First of all FIQ features a number of the banked registers is greater than IRQ, specifically devoted and not shared with others. This means that when it is necessary to perform a context switch FIQ will have immediately available a set of memory banks devoted to its management while in the other cases it is necessary to save them in a suitable area (stack) and after the service to recover them.

FIQ moreover vector is the last entry in the vector table. FIQ handler therefore can be placed directly at the vector location and run sequentially from that address without the need for a branch and its associated delays, since the length of the routine will be not limited by the next address of a location that contains the routine address for another interrupt service.

That's the last one! If the system has a cache, the vector table and FIQ handler may all be locked down in one block and this speeds further.

- Why the return address from a Data Abort is LR-8 and from FIQ/IRQ or Fetch abort is LR-4

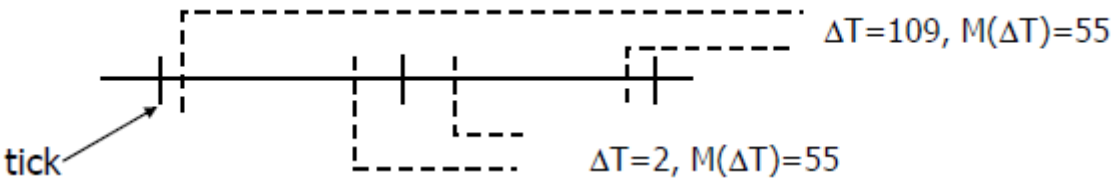
The Data Abort happens during the execution of the instruction when the third stage of the pipeline is active ("EXE") that is two instructions before the one actually fetched in the "FETCH" stage. Since an instruction is 32 bit long that is 4 bytes long to re-execute the instruction causing the DATA ABORT requires to load the PC with the content of the LINK REGISTER (that contains the PC) – 8.

Similarly the Fetch Abort occurs when an instruction is fetched from the memory and since the PC has been contemporaneously upgraded to PC+4 in case of Abort it is necessary to decrease it by "-4" to repeat the instruction.

Of course in both the cases the assumption is that when a "Abort" situation is noticed the system tries to correct it and to repeat the interrupted instruction.

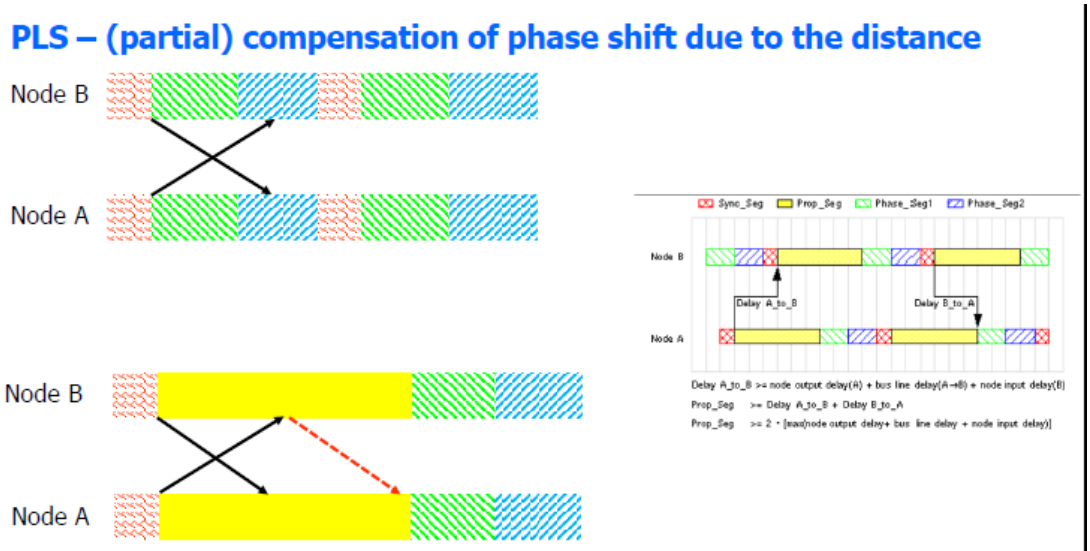
- Explain with an example what does it mean that events, whose time distance is N*BTL, can correspond to a real time interval that can range from (N-1) up to (N+1) UTL*BTL?

Let's consider the slide 56 of the "Digital Interfacing block" and in particular the figure that is shown



This picture shows two examples with events belonging to intervals that are consecutive therefore their time distance in the internal machine representation is M(ΔT). However in one case two events are very close to the tick that separates the wo intervals and therefore their real time distance is close to zero. In another case the two events are very far and close to the first tick and the last tick that is the tick that states the (N-1)BTL point and the tick that states the (N+1) BTL point therefore their real time distance is close to 2UTL*BTL

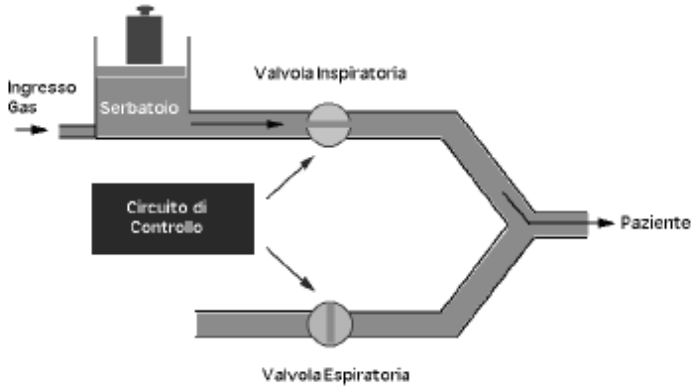
- In case we have PS1=PS2=2TQ in Can bus and a PTS=3TQ show what happens with and without PTS so demonstrating its utility.

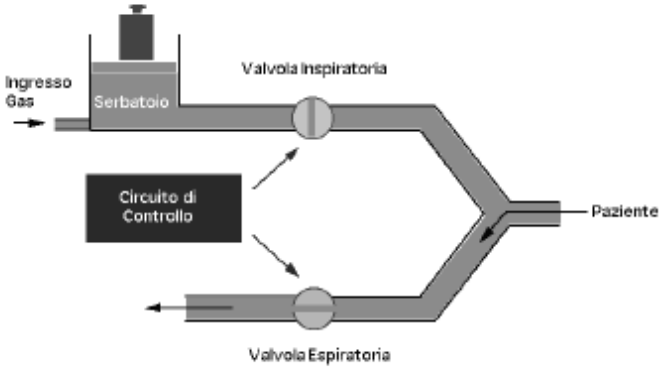


The picture shows the situation considered a part the specific values assigned to PS1, PS2 and PTS.

In the first case two nodes are in competition for the bus and their bits should be perceived at the same time so to understand who is the arbitration winner. However due to the distance skew the value of the bit of the other node could arrive after the sampling point so as every node is not able to understand if he has won or not the arbitration. In the second case the presence of a

suitable compensation block allows to move ahead the sampling point so as every node can check the bit status only when the bits have been effectively received. In the case required by the exercise the policy will work only if the time distance between the two nodes is equal to 3 TQs.





3. Respiratory failure is one of the most common complications related to COVID-19, the infection triggered by the new coronavirus that emerged in China. As many as 10 percent of affected patients need intensive care treatment, basically to be treated with mechanical ventilation or artificial ventilation and support their breathing. This life-saving procedure takes place through a medical device that is present in each intensive care unit (ICU): the pulmonary ventilator.

The pulmonary ventilator is a medical device that has the purpose of integrating or replacing the activity of the muscles related to breathing, i.e. the diaphragm and the intercostals. Simply put, the mechanical ventilator is a device designed to blow air (or gas mixtures) into the patient's lungs with a specific frequency and with finely calibrated pressures; stop insufflation and allow gas exchange between the alveoli and blood capillaries; promote exhalation with the release of gas (carbon dioxide) which occurs due to the elastic nature of the lungs; start a new cycle that allows to replicate in all respects the natural lung respiration. Modern lung ventilators automatically calculate the volume of air to be conveyed to the patient based on the recorded pressures.

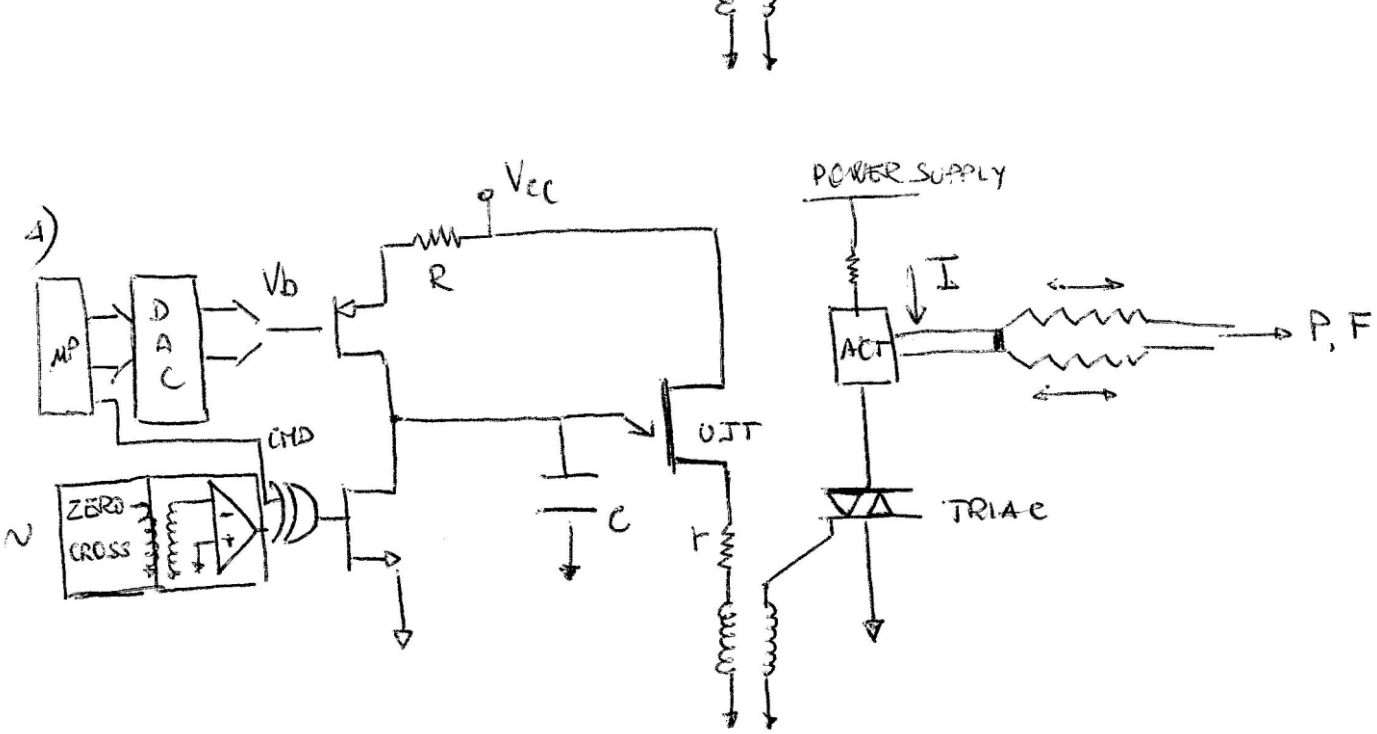
The air is blown into the rib cage through instruments that are typical of the so-called "intubation". The main one is the endotracheal tube, which is inserted into the patient's mouth and which, as its name suggests, passes through the trachea. In practice, trace the path to direct the air directly into the lungs. Intubation is always practiced after having put the patient to sleep, so he/she does not notice the insertion and removal of the tube, considered an invasive procedure.

The passage from the forced inspiratory phase to the expiratory one is obtained through the opening and closing of suitable valves as shown in the figure. The mixed air is blown into the lungs through a bellows pump (see figure) moved by an electromagnetic actuator and by monitoring the patient's ECG the frequency of the actuator is automatically adjusted based on the heart rate acquired.

How many bits are used by the microprocessor to measure the PV with a 2% precision and to drive the actuator together with the opening/closing holes of the valves?

The first group of bits is related to the measurement of the PV that in the text is said to be the ECG frequency. On the other hand this frequency must be put in relationship to the frequency of the air blowing that is the real variable that is monitored. Therefor we can think to measure the air flowrate with a flowmeter and to associate the ECG to it with a suitable look up table. Among the several flowmeters that we know we can choose those with an analog output (electromagnetic one for example) and in this case we will need 6 bits for the conversion plus 2 for the SoC/EoC commends. As an alternative we can choose flowmeters with digital output (i. e. with an incremental encoder) and in this case we will use only a couple of bits.

The actuator is electromagnetic and its movement is bidirectional, therefore we can drive it with a circuit including a TRIAC device. The picture shows a possible modification of the circuit we have seen at lesson.



In this case the microprocesscor will drive the DAC providing the Vb, therefore we can assume that this is done with the same precision as before that is 6 bits + 2 for SoC/EoC. Moreover we have to consider the CMD bit.

Concerning the valves they can be of two types: ON-OFF and in this case a suitable switch will be enough to drive them (that is a couple of MOS devices managed by a couple of bits, not only one because we need a pause between the closing of the first valve and the opening of the second one). As an alternative we can use gate-valves and in this case the opening/closing will be managed by a motor with a screw. If the motor is a stepper one we need bits to drive the power supply timer and the flip-flop regulator of the V13-V24 sequences. If the motor is DC we need to drive the motor with a circuit that is similar to the previous one with a TRIAC but in this case we need also a position transducer to measure the position of the valve (with a stepper motor the control is open-ring).